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EXAMINER	
HUANG, DAVID S	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,240	HSU ET AL.	
	Examiner	Art Unit	
	David Huang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,10,11,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,10,11,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, with respect to **claim 11** have been fully considered and are persuasive. The objection has been withdrawn.

2. Applicant's arguments, with respect to claims 2 and 11 have been fully considered and are persuasive. The 35 U.S.C. 112, 2nd paragraph, rejection has been withdrawn.

3. Applicant's arguments with respect to **claims 1, 2, 3, 4, 6, 10, 11, 21, and 22** have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

4. **Claims 2, 6 and 11** are objected to because of the following informalities:

In **claim 2**, line 8, "said first connection" is inconsistent with the rest of claim which seems to be directed to "a plurality of connection elements". For examination on the merits, the claim will be interpreted such that the second antifuse is part of one of the second connection elements, connecting the data transmitters to an input.

Claim 11 is dependent on claim 2 and contains the same defect.

Claim 6, lines 9 and 11 recite "said a low impedance state" and "said a high impedance state", respectively, but the "a" in both cases is unnecessary.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 1, 2, and 11** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 9-10, recite "a fuse" but it is unclear as to whether or not this limitation refers to the "a fuse" on line 5. For examination on the merits, the claim will be interpreted as best understood.

Claims 2 and 11 are dependent on claim 1, and contain the same defects

35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. **Claims 1, 2, 6, 11, and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shioka et al. (US 5,369,642) in view of Farnworth et al. (US 2003/0054592).

Regarding **claim 1**, Shioka et al. disclose an integrated circuit, comprising:

a plurality of output signal lines including a first output signal line (column 6, lines 26-33; 410, Figure 3);

a plurality of data transmitters including a plurality of default data transmitters and at least one redundancy data transmitter (DT 500-0 to 500-n, Figure 3); and

a plurality of connection elements (211 and 221, Figure 3) with first and second switches both with an electrically conductive state and an electrically high resistive state (R12 and R21, Figure 3), at least a first connection element of said plurality of connection elements having the first switch (R21, Figure 3) conductively connecting a first default data transmitter of said

plurality of default data transmitters to said first output signal line when the first switch is in said electrically conductive state and electrically disconnecting said first default data transmitter from said first output signal line when the first switch is in said electrically high resistive state, the second switch (R12, Figure 3) electrically disconnecting said redundancy data transmitter from said first output signal line when the second switch is in said electrically high resistive state and the second switch conductively connecting said redundancy data transmitter to said first output signal line when the second switch is in said electrically conductive state.

Shioka et al. fail to expressly disclose the connection elements each include a fuse and an antifuse that connect and disconnect the default and redundancy transmitters in the manner described above with the switches.

Farnworth et al. teaches fuses and anti-fuses are used to connect and disconnect defective units with redundant components in order to salvage otherwise defective components (page 2, [0021]; see Figure 3; it is inherent that fuses and anti-fuses both have conductive and high resistive states).

Because both Shioka et al. and Farnworth et al. teach means with conductive and high resistive states for connecting and disconnecting redundant components, it would have been obvious to one of ordinary skill in the art to substitute the fuses and anti-fuses of Farnworth et al. for the switches of Shioka for the obvious result of connecting redundant components in place of default components.

Regarding **claim 2**, Shioka et al. disclose everything claimed as applied to claim 1 above, and further disclose a plurality of second connection elements (210 and 220, Figure 3), including a switch having an electrically conductive state and an electrically high resistive state, at least

one of the switches conductively connecting said first default data transmitter to a first input signal line (column 6, lines 24-26; 400-1, Figure 3) when the switch is in said electrically conductive state and electrically disconnecting said first default data transmitter from said first input signal line when the switch is in said electrically high resistive state (R21, Figure 3), and also including a relay having an electrically high resistive state and an electrically conductive state, the relay electrically disconnecting said redundancy data transmitter from said first input signal line when the relay is in said electrically high resistive state and conductively connecting said redundancy data transmitter to said first input signal line when the relay is in said electrically conductive state (R12, Figure 3).

Shioka et al. fail to expressly disclose the connection elements each include a fuse and an antifuse that connect and disconnect the default and redundancy transmitters in the manner described above with the switches.

Farnworth et al. teaches fuses and anti-fuses are used to connect and disconnect defective units with redundant components in order to salvage otherwise defective components (page 2, [0021]; see Figure 3; it is inherent that fuses and anti-fuses both have conductive and high resistive states).

Because both Shioka et al. and Farnworth et al. teach means with conductive and high resistive states for connecting and disconnecting redundant components, it would have been obvious to one of ordinary skill in the art to substitute the fuses and anti-fuses of Farnworth et al. for the switches and relays of Shioka for the obvious result of connecting redundant components in place of default components.

Regarding **claim 11**, Shioka discloses everything claimed as applied above, further disclose in a separate embodiment each of said default data transmitters provides a pair of differential signal outputs and receives a pair of differential signal inputs, such that said first output signal line includes a pair of differential signal conductors for receiving said differential signal outputs and said first input signal line includes a pair of differential signal conductors for providing said differential signal inputs.

Specifically, Shioka et al. disclose signal lines 961 and 971 are each implemented as a balanced two-core cable whose impedance is equal to the characteristic impedance Z of the input signal sources 40-42 and DTs 50-52 connected to the input terminals 940-942 and output terminals 950-952 (column 3, lines 30-35). The switches and input and output terminals are each provided with a bipolar configuration (column 3, lines 1-3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the balanced two-core cable teaching of Shioka et al. since it provides impedance matching which eliminates waveform distortion and falling levels of the transmission signals (column 3, lines 27-30).

Regarding **claim 21**, Shioka et al. disclose an integrated circuit, comprising:

a plurality of output signal lines including a first output signal line (OS1 to OSn, 410-1 to 410-n, Figure 3);

a plurality of input signal lines including a first input signal line (IS1 to ISn, 400-1 to 400-n, Figure 3);

a plurality of data transmitters including a plurality of default data transmitters and at least one redundancy data transmitter (DT 500-0 to 500-n, Figure 3); and

a plurality of first connection elements (211 and 221, Figure 3) each including a first switch having an electrically conductive state and an electrically high resistive state, at least one of said first switches conductively connecting a first default data transmitter of said plurality of default data transmitters to said first output signal line when said first switch is in said electrically conductive state and electrically disconnecting said first default data transmitter from said first output signal line when said first switch is in said electrically high resistive state (R21, Figure 3; column 6, lines 15-19, 26-33); and

a plurality of second connection elements (210 and 220, Figure 3) each including a second switch having an electrically conductive state and an electrically high resistive state, at least one of said second switches conductively connecting said first default data transmitter to said first input signal line when said second switch is in said electrically conductive state and electrically disconnecting said first default data transmitter from said first input signal line when said second switch is in said electrically high resistive state (R21, Figure 3).

Shioka et al. fail to expressly disclose the connection elements each include a fuse and an antifuse that connect and disconnect the default and redundancy transmitters in the manner described above with the switches.

Farnworth et al. teaches fuses and anti-fuses are used to connect and disconnect defective units with redundant components in order to salvage otherwise defective components (page 2, [0021]; see Figure 3; it is inherent that fuses and anti-fuses both have conductive and high resistive states).

Because both Shioka et al. and Farnworth et al. teach means with conductive and high resistive states for connecting and disconnecting redundant components, it would have been obvious to one of ordinary skill in the art to substitute the fuses and anti-fuses of Farnworth et al. for the switches of Shioka for the obvious result of connecting redundant components in place of default components.

Regarding **claim 6**, Shioka et al. discloses everything claimed as applied to claim 21 above, and further disclose said first connection element (211, Figure 3) further includes a first relay (R12, Figure 3) and said second connection element (210, Figure 3) further includes a second relay (R12, Figure 3), wherein

said first relay conductively connects said redundancy transmitter to said first output signal line when said first relay is in a low impedance state and electrically disconnects said redundancy data transmitter from said first output signal line when said first relay is in a high impedance state (column 6, line 59-column 7, line 13) and

said second relay conductively connects said redundancy data transmitter to said first input signal line when said second relay is in said a low impedance state and electrically disconnects said redundancy data transmitter from said first input signal line when said second relay is in said a high impedance state (column 6, line 59-column 7, line 13).

Shioka et al. fail to expressly disclose the connection elements each include a fuse and an antifuse that connect and disconnect the default and redundancy transmitters in the manner described above with the switches.

Farnworth et al. teaches fuses and anti-fuses are used to connect and disconnect defective units with redundant components in order to salvage otherwise defective components (page 2,

[0021]; see Figure 3; it is inherent that fuses and anti-fuses both have conductive and high resistive states).

Because both Shioka et al. and Farnworth et al. teach means with conductive and high resistive states for connecting and disconnecting redundant components, it would have been obvious to one of ordinary skill in the art to substitute the fuses and anti-fuses of Farnworth et al. for the relays of Shioka for the obvious result of connecting redundant components in place of default components.

9. **Claims 22** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shioka et al. (US 5,369,642) in view of Maldanado (US 6,819,197).

Regarding **claim 22**, Shioka et al. disclose an integrated circuit comprising:

a plurality of output signal lines including a first output signal line (OS1 to OSn, 410-1 to 410-n, Figure 3);

a plurality of input signal lines including a first input signal line (IS1 to ISn, 400-1 to 400-n, Figure 3);

a plurality of data transmitters including a plurality of default data transmitters and at least one redundancy data transmitter (DT 500-0 to 500-n, Figure 3); and

a plurality of first connection elements (211 and 221, Figure 3) each including a first switch having an electrically conductive state and an electrically high resistive state, at least one of said first switches conductively connecting a first default data transmitter of said plurality of default data transmitters to said first output signal line when said first switch is in said electrically conductive state and electrically disconnecting said first default data transmitter from

said first output signal line when said first switch is in said electrically high resistive state (R21, Figure 3; column 6, lines 15-19, 26-33); and

a plurality of second connection elements (210 and 220, Figure 3) each including a second switch having an electrically conductive state and electrically high resistive state, at least one of said second switches conductively connecting said first default data transmitter to said first input signal line when said second switch is in said electrically conductive state and electrically disconnecting said first default data transmitter from said first input signal line when said second switch is in said electrically high resistive state (R21, Figure 3).

Shioka et al. fail to expressly disclose the first and second switches are MEM switches.

However, Maldonado teaches MEM switches are well known in the art to be used in place of mechanical or other semiconductor switches as evidenced by Maldonado (column 7, lines 31-35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide MEM switches for circuit taught by Shioka et al. since MEM switches are well known in the art to be used in place of mechanical or other semiconductor switches.

10. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shioka et al. (US 5,369,642) in view of Maldanado (US 6,819,197) as applied to claim 22 above, and further in view of Sun et al. (US Patent 6,307,169).

Regarding **claim 10**, Shioka et al. disclose everything claimed as applied to claim 22 above, but fails to expressly disclose wherein said plurality of MEM switches include MEM switches of the type having a signal pad restrained by a plurality of hinge brackets for movement

in a substantially vertical direction in response to electrostatic force to switch between a connecting state and a disconnecting state.

Sun et al. disclose a MEMS switch having a double hinge membrane-type control electrode with center flex. Each end of the electrode is hinged or anchored to a post, spacer , via or other type of stationary vertical structure. Thus, when the appropriate voltage is applied between the two control electrodes, the membrane-type hinged electrode flexes as the center, i.e., between the two hinges, in the direction of the opposite electrode. When the voltage is removed., the natural resiliency of the membrane-type electrode returns it to its normally horizontal, open state (column 1, lines 25-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the combination of Shioka et al. and Maldonado with the MEMS switch taught by Sun et al. since it reduces power consumption by using the natural resiliency of the membrane to change to an open state(column 1 lines 35-38).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Huang whose telephone number is (571) 270-1798. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSH/dsh
1/21/2008

SHUWANG LIU
SUPERVISORY PATENT EXAMINER